CLAIMS

What is claimed is:

1. A method of placing a circuit design comprising a component having input signals with asymmetric delays, the method comprising the steps of:

determining an arrival time for each input signal of a plurality of input signals to the component ;

identifying a propagation delay associated with each input port of a plurality of input ports of the component ; and

ordering the plurality of input signals of the component according to the arrival times and the propagation delays.

2. The method of claim 1, further comprising first identifying topological levels of the circuit design.

3. The method of claim 2, further comprising repeating said determining, said identifying, and said ordering steps for each component within an identified topological level.

4. The method of claim 3, further comprising iteratively performing said repeating step for each identified topological level of the circuit design.

5. The method of claim 4, wherein the topological levels are processed in hierarchical order.

6. The method of claim 5, further comprising updating timing information for the circuit design after ordering input signals of each component of an identified topological level.

7. The method of claim 1, said ordering step further comprising the step of matching input signals having an

earlier arrival time with input ports of the component having longer propagation delays.

8. The method of claim 7, wherein said matching step matches a first input signal having an earliest arrival time with a first input port of the component having a longest propagation delay, and a second input signal having a latest arrival time with an input port of the component having a shortest propagation delay.

9. The method of claim 1, said ordering step comprising:

sorting input signals according to an arrival time at the component;

sorting input ports of the component according to propagation delay; and

matching input signals having an earlier arrival time with input ports of the component having longer propagation delays.

10. The method of claim 9, wherein said matching step matches an input signal having an earliest arrival time with an input port of the component having a longest propagation delay, and an input signal having a latest arrival time with an input port of the component having a shortest propagation delay.

11. The method of claim 1 wherein the component is a look-up table (LUT).

12. A system for placing a circuit design comprising:

means for determining an arrival time for each input signal to a component within a circuit design representation;

means for identifying the propagation delay associated with each pin of the component; and

means for ordering input signals of the component according to the arrival times of each input signal and the

propagation delay of each pin of the component.

13. The system of claim 12, wherein the component is a look up table.

14. The system of claim 12, further comprising means for first identifying topological levels of the circuit design, and means for causing said means for determining, said means for identifying, and said means for ordering to operate on each component within an identified topological level.

15. The system of claim 13, further comprising means for iteratively processing each identified topological level of the circuit design representation, wherein said means for iteratively processing processes the topological levels in hierarchical order.

16. The system of claim 15, further comprising means for updating timing information for the circuit design representation after ordering input signals of each component of an identified topological level.

17. The system of claim 12, said means for ordering further comprising means for matching input signals having an earlier arrival time with pins of the component having longer propagation delays.

18. The system of claim 17, wherein said means for matching matches an input signal having an earliest arrival time with a pin of the component having a longest propagation delay, and an input signal having a latest arrival time with a pin of the component having a shortest propagation delay.

19. The system of claim 12, said means for ordering further comprising:

means for sorting input signals according to an arrival

time at the component;

means for sorting pins of the component according to propagation delay; and

means for matching input signals having an earlier arrival time with pins of the component having longer propagation delays.

20. The system of claim 19, wherein said means for matching matches an input signal having an earliest arrival time with a pin of the component having a longest propagation delay, and an input signal having a latest arrival time with a pin of the component having a shortest propagation delay.

21. A machine readable storage, having stored thereon a computer program having a plurality of code sections executable by a machine for causing the machine to perform the steps of:

determining an arrival time for each input signal to a look up table within a circuit design representation;

identifying the propagation delay associated with each pin of the look up table; and

ordering input signals of the lookup table according to the arrival times of each input signal and the propagation delay of each pin of the look up table.

22. The machine readable storage of claim 21, further causing the machine to perform the step of first identifying topological levels of the circuit design representation.

23. The machine readable storage of claim 22, further causing the machine to perform the step of repeating said determining, said identifying, and said ordering steps for each look up table within an identified topological level.

24. The machine readable storage of claim 23, further causing the machine to perform the step of iteratively

performing said repeating step for each identified topological level of the circuit design representation.

25. The machine readable storage of claim 24, wherein the topological levels are processed in hierarchical order.

26. The machine readable storage of claim 25, further causing the machine to perform the step of updating timing information for the circuit design representation after ordering input signals of each look up table of an identified topological level.

27. The machine readable storage of claim 21, said ordering step further comprising the step of matching input signals having an earlier arrival time with pins of the lookup table having longer propagation delays.

28. The machine readable storage of claim 27, wherein said matching step matches an input signal having an earliest arrival time with a pin of the lookup table having a longest propagation delay, and an input signal having a latest arrival time with a pin of the lookup table having a shortest propagation delay.

29. The machine readable storage of claim 21, said ordering step comprising:

sorting input signals according to an arrival time at the look up table;

sorting pins of the look up table according to propagation delay; and

matching input signals having an earlier arrival time with pins of the look up table having longer propagation delays.

30. The machine readable storage of claim 29, wherein said matching step matches an input signal having an earliest

arrival time with a pin of the lookup table having a longest propagation delay, and an input signal having a latest arrival time with a pin of the lookup table having a shortest propagation delay.